


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)

Scholar [All articles](#) - [Recent articles](#) Results 1 - 10 of about 7,820 for **device address bit reorder**. (1

All Results

[T Tran](#)
[A Shamir](#)
[T Austin](#)
[E Tromer](#)
[S Hauck](#)

[... a command to a memory having a **reorder** module for priority commands and an arbiter tracking **address** ... - all 3 versions »](#)

DJ Harriman, BK Langendorf, RJ Riesenman - US Patent 6,112,265, 2000 - Google Patents
 ... for issue that specifies a memory **address** matching an ... in the same order in which the **device** issued the ... are available, ie have associated valid **bits** 274 reset. ...

[Cited by 22](#) - [Related Articles](#) - [Web Search](#)

[... and method for resolving dependencies among a plurality of instructions within a storage **device** - all 3 versions »](#)

TM Tran... - US Patent 5,345,569, 1994 - Google Patents

... **device** which provide a tag identifying matched desti- ... **address** ** d ° a ° ** **address** b tween * he of **reorder** buffer 22 for dependency checking. ...

[Cited by 70](#) - [Related Articles](#) - [Web Search](#)

[Solid state storage **device** - all 2 versions »](#)

EC Fromm, ML Anderson, LR Heidtke - US Patent 5,321,697, 1994 - Google Patents

... Daniel J. Kluth [57] ABSTRACT An improved solid state storage **device** (SSD) with ... A matrix **reorder** circuit is used to distribute data across individual memory ...

[Cited by 11](#) - [Related Articles](#) - [Web Search](#)

[Storage **device** having varying access times and a superscalar microprocessor employing the same - all 3 versions »](#)

TM Tran... - US Patent 5,900,012, 1999 - Google Patents

... equal to a respective number of high order **bits** of ... hold register 62 provide a temporary storage **device** for a ... line for the case where a request **address** misses ...

[Cited by 7](#) - [Related Articles](#) - [Web Search](#)

[INTERMEDIATE SPEED STORE LOW SPEED STORE DIRECTORR](#)

US Patent 3,737,881, 1973 - Google Patents

... been searched (the logical 1 **bit** is again in position 1 ... a symbolic ad -dress and a physical **address** for pages of data stored in the **device**, each register ...

[Cited by 14](#) - [Related Articles](#) - [Web Search](#)

[Data processing **device** with memory coupling unit - all 3 versions »](#)

RG Fleck, K Oberlaender, G Baror, A Eder - US Patent 6,405,273, 2002 - Google Patents

... (54) DATA PROCESSING **DEVICE** WITH MEMORY ... A memory having a plurality of n-**bit**

input/output ports ... the memory with the register file, a memory **address** and select ...

[Cited by 5](#) - [Related Articles](#) - [Web Search](#)

[\[PDF\] High-bandwidth **address** translation for multiple-issue processors - all 4 versions »](#)

TM Austin, GS Sohi - ISCA, 1996 - minds.wisconsin.edu

... banks, and hence, the band- width delivered by the **device**. In our evaluations, we consider both **bit** selection, which ... a portion of the virtual page **address** to se ...

[Cited by 27](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

Cited by 4 - Related Articles - Web Search

Cited by 2 - Related Articles - Web Search

Cited by 13 - Related Articles - Web Search



Result Page: **1** 2 3 4 5 6 7 8 9 10 **Next**

device address bit reorder Search

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2007 Google


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

device address bit reorder

Search

[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)
Scholar [All articles](#) - [Recent articles](#) Results 11 - 20 of about 7,820 for **device address bit reorder**.
All Results[T Tran](#)[A Shamir](#)[T Austin](#)[E Tromer](#)[S Hauck](#)**Reorder buffer employing last in buffer and last in line bits - all 2 versions »**

TM Tran, DB Witt... - US Patent 5,768,555, 1998 - Google Patents

... I/O **Device** I/O **Device** FIG. 10 208 ... Microprocessors which implement out of order executionBUFFER AND LAST IN LINE **BITS** often employ a **reorder** buffer for ...[Cited by 15](#) - [Related Articles](#) - [Web Search](#)**Factoring Large Numbers with the TWIRL Device - all 13 versions »**

A Shamir, E Tromer - Advances in Cryptology-CRYPTO 2003: 23rd Annual ..., 2003 - books.google.com

... We **address** this with a heterogeft9et 4esign that uses ... estimates suggest that for 1024-**bit** composites the ... 2 reviews the sieving problem and the TWINKLE **device**. ...[Cited by 54](#) - [Related Articles](#) - [Web Search](#)**Flexible graphics interface device switch selectable big and little endian modes, systems and ... - all 3 versions »**

JR Van Aken, CJ Yin - US Patent 5,446,482, 1995 - Google Patents

... [54] FLEXIBLE GRAPHICS INTERFACE **DEVICE** SWITCH SELECTABLE BIG ... and includes an arrayof jsequentially ordered data input terminals for receiving aj-**bit** word of ...[Cited by 17](#) - [Related Articles](#) - [Web Search](#)**A Novel Scatternet Scheme with IPv6 Compatibility - all 3 versions »**

WK Lai, DH Tan - Mobile Networks and Applications, 2003 - Springer

... Current node Ext C/S **Reorder** Length Forward Routing Vector s1 ... The unique Bluetooth **Device Address** formed by the ... last 48 **bits** can be used to distinguish between ...[Cited by 1](#) - [Related Articles](#) - [Web Search](#)**Data processing system with reorganization of disk storage for improved paging - all 3 versions »**

TA Kriz - US Patent 4,680,703, 1987 - Google Patents

... these **bits** are reset, so the **bit** distinguishes between ... between tracks of a disk storage **device** and page ... memory, including means for selecting a track **address**, ...[Cited by 13](#) - [Related Articles](#) - [Web Search](#)**Semiconductor memory device having row and column redundancy circuit and method of manufacturing the ... - all 3 versions »**

T Bhm, H Kandolf, S Lammers, Z Manyoki - US Patent 6,618,306, 2003 - Google Patents

... **device**, only when the first control **bit** has a given first binary value, setting a first operating state in which the **address** decoding **device** uses **bits** of all ...[Cited by 1](#) - [Related Articles](#) - [Web Search](#)**Method and apparatus for saving the effective address of floating point memory operations in an out- ... - all 3 versions »**

AF Glew, JM Abramson, KG Konigsfeld, A Bajwa, WR ... - US Patent 5,721,857, 1998 - Google Patents

... the location designators of the ROB (**Reorder** Buffer) to ... and error pointers consisting

of two 16-bit registers operand **address** (if present) in registers mat can ...

[Cited by 11](#) - [Related Articles](#) - [Web Search](#)

Apparatus and method for modifying status bits in a reorder buffer with a large speculative state - all 3 versions »

TC Tan, TM Tran... - US Patent 5,920,710, 1999 - Google Patents

... I/O **Device** 206N 208 FIG. 12 Main Memory 204 200 Page 14. 5,920,710 APPARATUS AND

METHOD FOR MODIFYING STATUS BITS IN A REORDER BUFFER WITH A LARGE SPECULATIVE ...

[Cited by 4](#) - [Related Articles](#) - [Web Search](#)

Sequential nibble burst ordering for data - all 8 versions »

JW Janzen - US Patent 7,085,912, 2006 - Google Patents

... However, double sided memory **device** outputting data to the ... ie, **reorder**) must be performed on the 4 bit ... The command, **address**, and clock signal lines 134, 132 ...

[Cited by 2](#) - [Related Articles](#) - [Web Search](#)

Memory device having different burst order addressing for read and write operations - all 7 versions »

JW Janzen - US Patent 7,082,491, 2006 - Google Patents

... 2. The **device** of claim 1 wherein said **reorder** circuit is configured for examining at least two of the least significant **bits** of a column **address** and wherein ...

[Related Articles](#) - [Web Search](#)



Result Page: [Previous](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [Next](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2007 Google


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

bit reorder address

Search

[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)
Scholar All articles - **Recent articles** Results 1 - 10 of about 15,000 for **bit reorder address**. (0.25 s)
All Results[D Hunt](#)[A Kumar](#)[T Tran](#)[D Witt](#)[J Garside](#)**Advanced performance features of the 64-bit PA-8000 - all 4 versions »**

D Hunt - Compcon'95. 'Technologies for the Information Superhighway', ..., 1995 -
 ieexplore.ieee.org

... s first CPU to implement the new 64-bit PA2.0 ... are a fifty-six entry instruction **reorder**
 buffer to ... out-of-order execution, a branch target **address** cache, branch ...

Cited by 109 - [Related Articles](#) - [Web Search](#)

... a command to a memory having a reorder module for priority commands and an arbiter tracking address ... - all 3 versions »

DJ Harriman, BK Langendorf, RJ Riesenman - US Patent 6,112,265, 2000 - Google Patents
 ... For example, valid data **bit** 274' is set when data is ... command select logic 240 selects
 a command from **reorder** slots 230 targeted to an **address** in memory 120 ...

Cited by 22 - [Related Articles](#) - [Web Search](#)

A 56-entry instruction reorder buffer

NB Gaddis, JR Butler, A Kumar, WJ Queen - Solid-State Circuits Conference, 1996. Digest of
 Technical ..., 1996 - ieexplore.ieee.org

... to the index of each reference active in the 28-entry **address reorder** buffer (AIRB ...
 The solution is the comparator **bit** slice circuit in Figure 3. This circuit ...

Cited by 22 - [Related Articles](#) - [Web Search](#)

Apparatus and method for resolving dependencies among a plurality of instructions within a storage ... - all 3 versions »

TM Tran... - US Patent 5,345,569, 1994 - Google Patents

... conditions, processor order" by the decoder as allowed by the **reorder** buffer,
 states, and the **address** of the current instruction to In ...

Cited by 70 - [Related Articles](#) - [Web Search](#)

Reorder buffer circuit accommodating special instructions operating on odd-width results - all 3 versions »

BD McMinn, RD Gowin Jr... - US Patent 5,727,177, 1998 - Google Patents

... cir- generates a result having a large **bit**-width size, the large ... supplying cuity
 may not increment the **reorder** buffer **address** suffi- instructions ...

Cited by 7 - [Related Articles](#) - [Web Search](#)

[PDF] Exploiting Bit-Slice Inactivities for Reducing Energy Requirements of Superscalar Processors - all 6 versions »

K Ghose, D Ponomarev, G Kucuk, A Flinders, P Kogge ... - Proc. of Kool Chips Workshop,
 Micro-33, 2000 - opal.cs.binghamton.edu

... register files, instruction dispatch buffers, **re-order** buffers, as well ... units or
 moved into the **reorder** and dispatch ... with the use of **bit**-value invariances ...

Cited by 10 - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

The HP PA-8000 RISC CPU - all 5 versions »

A Kumar - Micro, IEEE, 1997 - ieexplore.ieee.org

... System bus interface Runway bus 64-bit integer ALUs Shift/ merge units ... Memory buffer
 (28 entries) **Address reorder** buffer 28 entries Instruction cache ...


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

bit reorder address

Search

[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)
Scholar All articles - **Recent articles** Results 11 - 20 of about 15,000 for bit reorder address. (0.12 :
All Results[D Hunt](#)[A Kumar](#)[T Tran](#)[D Witt](#)[J Garside](#)**[PDF] 32-Bit RISC Pipelined Processor**

A Bhatt, A Dhanotia, MD CharuSachdeva, N Choudary, ... - cadence.co.in

... The processor is a 32 – **bit** Load/Store architecture where ... memory or the register file from the **reorder** buffer on ... back is not performed and the **address** of the ...[Related Articles](#) - [View as HTML](#) - [Web Search](#)**[Context-switched multi-stream pipelined reorder engine - all 2 versions »](#)**

R Rahim, V Talapaneni, PG Lacroute - US Patent 7,085,274, 2006 - Google Patents

... from Fig. 7B Update Rptr array and valid **bit** array. Read up to two entries from **reorder** buffer. Read notification assembly memory. Calculate offset **address(s)** ...[Web Search](#)**[ance Features of the 64-bit PA-8000 - all 2 versions »](#)**

D Hunt - doi.ieeeecs.org

... s first CPU to implement the new 64-**bit** PA2.0 ... are a fifty-six entry instruction **reorder** buffer to ... out-of-order execution, a branch target **address** cache, branch ...[Related Articles](#) - [Web Search](#)**[Reorder engine with error recovery - all 3 versions »](#)**

R Rahim - US Patent 7,209,482, 2007 - Google Patents

... Ifthe valid **bit** is set for the cell corresponding to Rptr, **reorder** engine 322 processes that cell by outputting the cell **address** for the cell (acts 603 and ...[Related Articles](#) - [Web Search](#)**[VLSI implementation of programmable FFT architectures for OFDM communication system](#)**

SY Lee, CC Chen - International Conference On Communications And Mobile ..., 2006 - portal.acm.org

... are utilized as **address** control for different column paths in the recursive-based shared- memory based architecture. Moreover, the **bit reorder** is required to ...[Related Articles](#) - [Web Search](#)**[Design considerations for 32-bit microprocessor TX3](#)**

K Okamoto, M Miyata, H Kishigami, T Miyamori, T ... - Compcon Spring'88. Thirty-Third IEEE Computer Society ... - ieeeexplore.ieee.org

... two General Register Files and the **Reorder** Buffer [9 ... The MMU includes the **Address** Generator and the TLB ... also complex in- structions such as **bit** field instructions ...[Cited by 1](#) - [Related Articles](#) - [Web Search](#)**[Energy-Efficient Design of the Reorder Buffer - all 7 versions »](#)**

D Ponomarev, G Kucuk, K Ghose - Proc. 12th Int'l Workshop Power and Timing Modeling, ..., 2002 - Springer

... Energy-Efficient Design of the **Reorder** Buffer 291 ... that each ROB entry may hold only a 32-**bit** long result ... Every ROB entry contains a field for the **address** of the ...[Cited by 11](#) - [Related Articles](#) - [Web Search](#)**[Random access memory with access on bit boundaries - all 2 versions »](#)**

BD Mandalia - US Patent 5,121,354, 1992 - Google Patents

... 40 respond to the same **bit** boundary code to **reorder** the data in ... 0 signals on lines B1-B6 to access **bit** cells of ... 7-16 in the array 30 at the **address** selected by ...

[Cited by 9](#) - [Related Articles](#) - [Web Search](#)

[\[PDF\] P4 Out-of-order execution unit and comparison to POWER4 - all 2 versions »](#)

J Manton - csil.cs.uiuc.edu

... each logical processor can use up to a maximum of 63 **re-order** buffer entries ... P4 is 32-**bit**, POWER4 is 64-**bit** machine Page 8. ... General-purpose **Reorder** Buffer (ROB ...

[Related Articles](#) - [View as HTML](#) - [Web Search](#)

[Residential fuel-oil level reporting and alarm system - all 3 versions »](#)

JD Knight, RD Shapiro, FH Banks, A Mitchell, BS ... - US Patent 4,845,486, 1989 - Google Patents

... m **ADDRESS** DECODING i CONTROL LOGIC ... determines the time duration of each **bit** by averaging

45 located at ... ates a **reorder** signal when the fuel-oil level in tank 104 ...

[Cited by 27](#) - [Related Articles](#) - [Web Search](#)



Result Page: [Previous](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [Next](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2007 Google